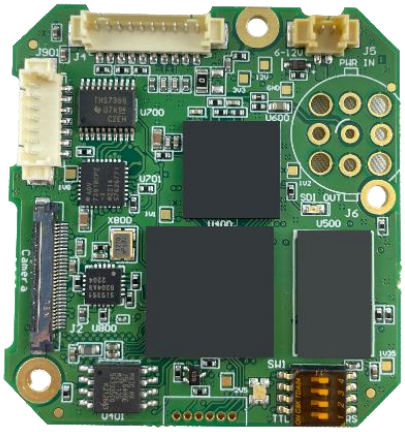
3G/HD-SDI Premium

Technical Manual



P/N – TV10 0090: 3G/HD-SDI **Premium** interface board for LVDS zoom cameras

P/N – TV50 0020: Mounting kit for TV10 0090 - 3G/HD-SDI Premium I/F boards
Includes: 30-way micro-coax camera cable, 2-way cable (power supply), 10-way cable (RS232/TTL/Analog output), 7-way cable (GPIOs), right angle black anodized bracket, screws and spacers

P/N – TV50 0021: Cable kit for TV10 0090 - 3G/HD SDI Premium I/F boards
Includes: 30-way micro-coax camera cable, 2-way cable (power supply), 10-way cable (RS232/TTL/Analog output)

Available connectors: VOPTEM02 (MCX connector), VOPTEM03 (SMB connector), VOPTEM04 (No connector)

Table of content

Revision History

Date	Revision	Description	Modified by	Note
07/02/23	A	Creation of the document	CBO	
19/01/24	B	Document refactoring	CBO	
12/06/24	C	Add REG_CAM_UART_BYPASS Change DIP switch video format Change SD input format needed	CBO	

Key features

- 3G-SDI SMPTE 424M, HD-SDI 292 M
- Video resolution up to 1080p60
- Analog video output selectable:
  - Composite video (CVBS)
  - S-Video (Y/C)
  - Component video (YPbPr colorspace)
- PAL and NTSC compliant output with multiple format possibilities: Letter box, Squeeze or Crop
- Communication UART – RS232/TTL using VISCA
- Setup & Update via UART
- Video mode selection by DIP switches
- Power supply 7V-12VDC
- Consumption under 6W with camera
- Automatic LVDS & format camera recognition
- Add-on connector for custom functionalities
- Operating temperature [0°C; 60°C]

General description

3G-SDI technology is the first established standard providing sufficient bandwidth to transmit uncompressed high-definition video signals from camera to screen.

Using coaxial cables with very low power loss, enables video transmission over 100 meters. This distance can be increased up to 300 meters using equalization at the receiver.

The 3G-SDI Premium converts the native LVDS video signal from camera blocks to 3G-SDI. It takes advantage of a high quality, low jitter, and uncompressed SDI stream.

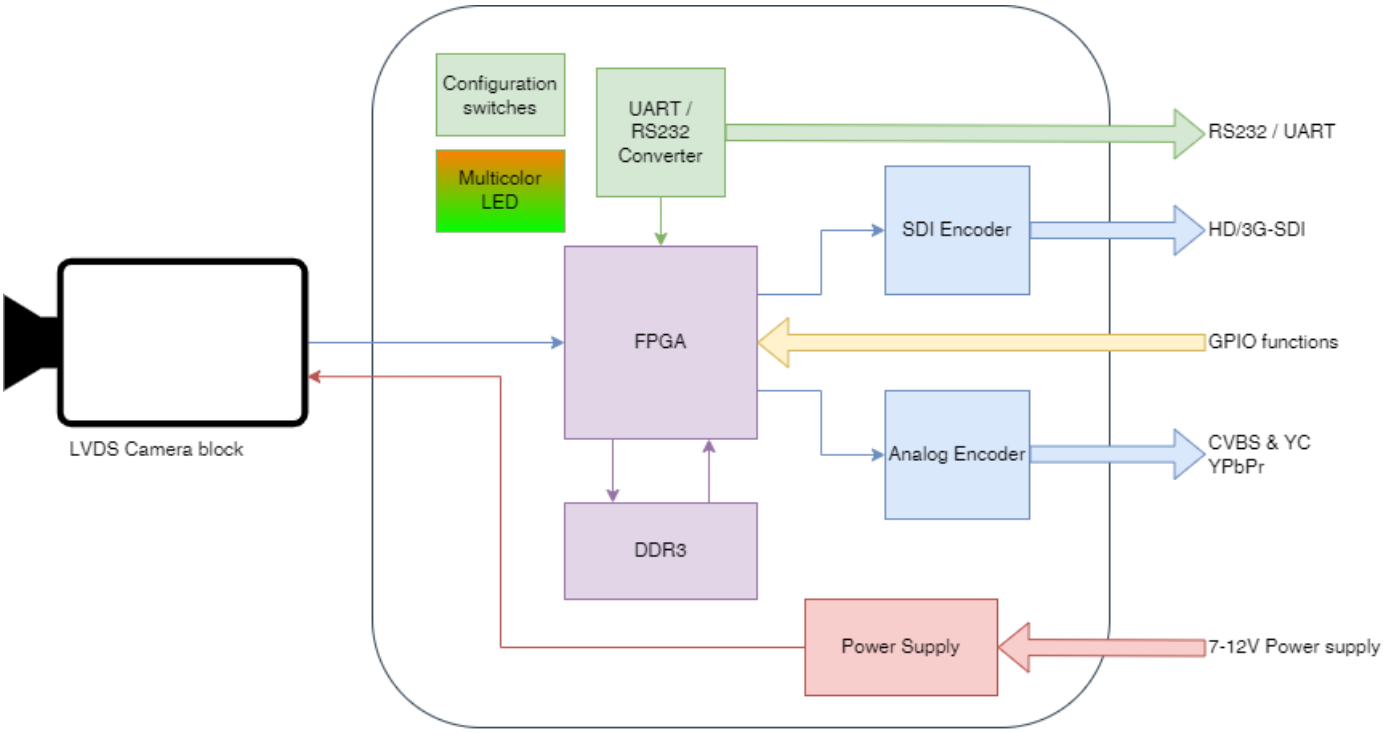
The Premium board has an additional analog output which is perfect to conserve your already-in-use analog system. The dual output 3G and analog will significantly reduce the number of boards, improving the cost and time-to-market. The 3G-SDI Premium module is based on a FPGA associated with DDR3 memory. Combined with i2S's expertise, complex image processing functions can be embedded on real time video flow such as colorimetry tests, measurements, reticules, contrast enhancement, ROI extraction, OSD and even more functions to fit your applications.

The add-on connector on the back side offers an infinity of new functionalities. The 3G-SDI Premium can be directly mounted into your system/end-products (plug-in) or connected to custom designed add-on board. Integrated RTC, audio embedded to SDI, second video input are some examples of the new possibilities / range of functionalities.

Benefits of this solution

- One single board, two simultaneous video outputs (3G-SDI and analog)
- Analog output generated even if the camera does not provide analog format
- RS232 / TTL serial communication easy switch
- Always keep up to date with an easy software update
- Addon connector for custom needs
- 3G SDI output connector choice between BNC, MCX and SMB
- GPIOs connector to easily send basic VISCA commands (zoom in / out, freeze on / off, focus)

Block diagram



Video acquisition

The main components are the FPGA for video acquisition and the DDR3 for video processing.
The board acquire LVDS video from the camera block with no latency deserialization to provide uncompressed 3G-SDI video output via an SDI converter.
The DDR3 allows high speed image processing for analog video output in CVBS, Y/C or YPbPr. Real time scaling to allow 4:3 SD video in Letterbox, Squeeze or Crop mode is available.

Communication

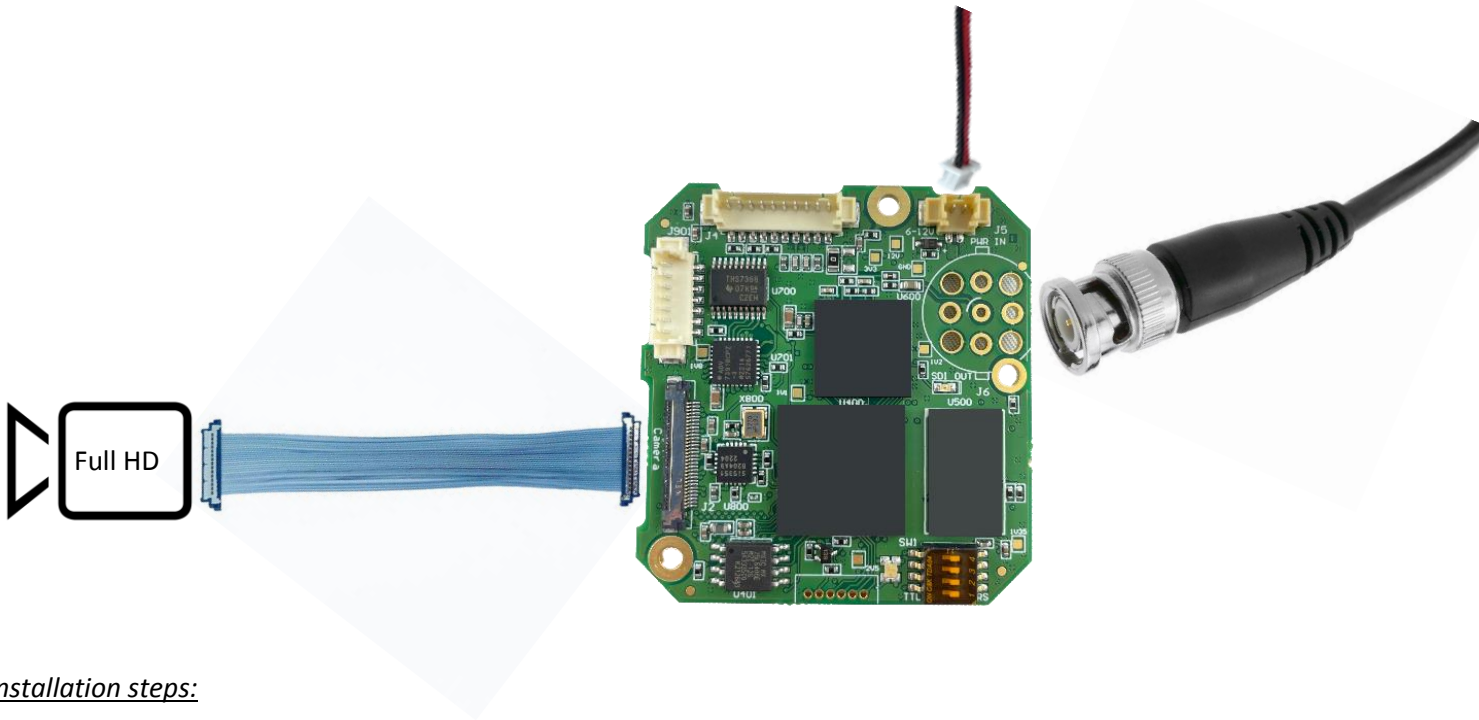
An UART / RS232 converter allows the user to select RS232 or UART TTL 3V3 communication. It is easily selectable via a DIP switch.
The DIP switch is used to manage the camera video format too.
A multicolor LED helps to know in which state the board is, it is quick feedback to be sure no error happened.

Power supply

The power input through the 2 ways connector J5 supports from 7V to 12V (1,5A). The camera is powered by the board.
The board is protected against shortcut and reversed cables.

Accessing to the video

Quick setup



Installation steps:

1. Connect the KEL cable between the board J2 and the camera.
2. Connect the SDI cable to the output connector of the board J6 and to the SDI monitor.
3. Connect the 2 ways power supply cable on J5 connector. Power input of the board is 7V to 12V (1,5A), red wire is for V+ and black wire is for the ground.
4. Now you can power the board.

Video characteristics

Introduction on video formats

You have two video format types:

- Progressive: displays both the even and odd scan lines (the entire video frame) at the same time. The video formats are listed with the letter ‘p’.
- Interlaced: displays even and odd scan lines as separate fields. The even scan lines are drawn on the screen, then the odd scan lines are drawn on the screen. Two of these even and odd scan line fields make up one video frame. The video formats are listed with the letter ‘i’.

Notion of LVDS mode: it is controlled by the register 74 of the camera (0x00: Single mode, 0x01: Dual mode). It is used to increase the video output from 4x LVDS data lines to 8x LVDS data lines. The output clock frequency is still 74,25MHz but with twice more date lanes. It is needed to process video formats 1080p50, 1080p59.94 and 1080p60.

If the camera itself does not have 4x additional LVDS data lanes, it will output data at 148,5MHz for video formats 1080p50, 1080p59.94 and 1080p60.

On LVDS full HD cameras blocks you can have several video formats available:

- Ful HD Interlaced 1920x1080i: it can be at 50, 59.94 or 60 FPS, the camera must be in Single mode.
- Full HD Progressive 1920x1080p: it can be at 25, 29.97 or 30 FPS, the camera must be in Single mode. It can also be at 50, 59.94 or 60 FPS, with these video formats only, the camera must be in Dual mode to be able to send more data.
- HD Progressive 1280x720p: it can be at 25, 29.97, 30, 50, 59.94 or 60 FPS, the camera must be in single mode.

LVDS video input supported resolutions

The video format from the LVDS camera can be configured by sending VISCA command (register 72) or by using the DIP switch of the board.
Please note that a Black & White pattern will be displayed if the input video format is not supported or not found.

	25	*29.97*	*30*	*50*	*59.94*	*60*
1280x720p	√	√	√	√	√	√
1920x1080p	√	√	√	√*	√*	√*
1920x1080i				√	√	√

* The video formats 1080p50, 1080p59.94 and 1080p60 require the camera configured in dual lane: register 74 set to 0x01. The others video formats require the register 74 set to 0x00 for single lane.

SDI video output

The output is an 8-bit SDI signal 800mV pp with 75-ohm impedance. It is compliant with SMPTE 424M (3G-SDI) and SMPTE 292M (HD-SDI). The output video format is the same as the camera (see LVDS video input resolutions supported upper).
Different output connector types are available: BNC, SMB or MCX. Please specify the connector you need in the order.

BNC  MCX  SMB 

Analog video output

The analog video output is selectable:

- analog SD:
  - Composite video (CVBS)
  - S-video (Y/C)
- analog HD:
  - Component video (YPbPr).

The selection is done via internal registers (REG_SD_FORMAT 0x20). The analog video output is available on a 10-pin molex connector.

According to the analog format you selected you must set the camera in specific video format:

Output video format	Analog HD (YPbPr)	Analog SD (CVBS)	Analog SD (Y/C)
Input video format supported	✓ 720p50 ✓ 720p59,94 ✓ 720p60 ✓ 1080p25 ✓ 1080p29,97 ✓ 1080p30	PAL or NTSC output: ✓ 720p50 ✓ 720p59,94 ✓ 720p60 ✓ 1080p25 ✓ 1080p29,97 ✓ 1080p30 ✓ 1080p50 ✓ 1080p59,94 ✓ 1080p60	PAL or NTSC output: ✓ 720p50 ✓ 720p59,94 ✓ 720p60 ✓ 1080p25 ✓ 1080p29,97 ✓ 1080p30 ✓ 1080p50 ✓ 1080p59,94 ✓ 1080p60

Analog SD video output quality can depend on the camera aperture configuration. Please refer to the datasheet of your camera and use the command “CAM_Aperture” to optimize the video quality.

Please note that the PAL or NTSC format is controlled by the register REG_SD_FPS 0x21.

3 modes can be selected via internal registers in analog SD 4:3:

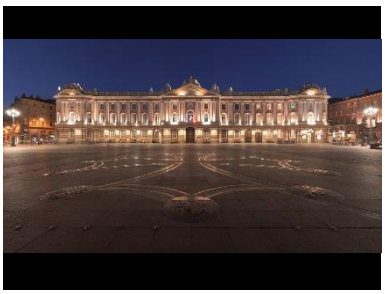


Figure 1: Letterbox

Figure 2: Squeeze

Figure 3: Crop

System configuration

Communication

Communication with the camera can be done through J4 connector. For the connector pinout please see paragraph Connectors.

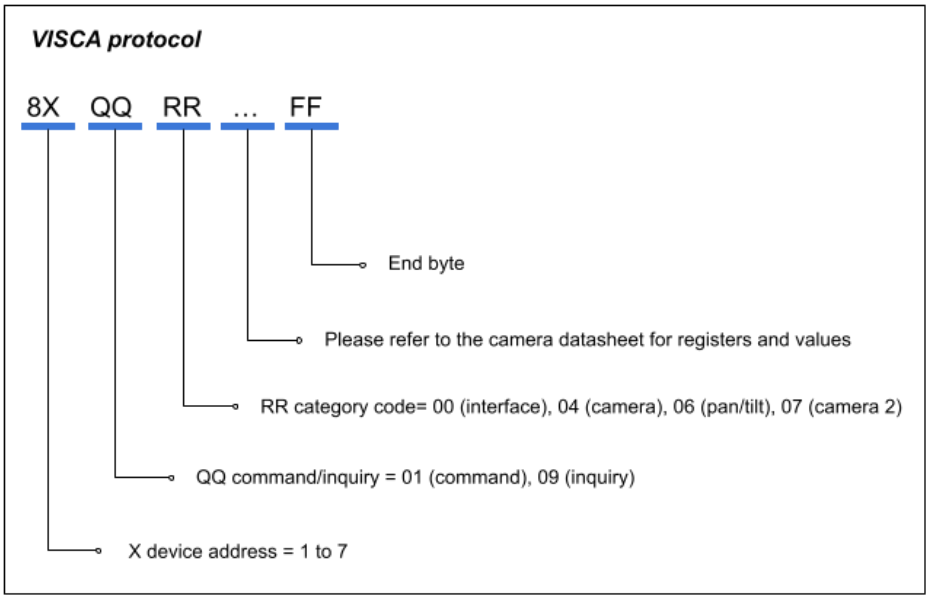
Communication can be set to either RS232 mode (according to EIA RS-232 specification) or TTL mode (UART with 3.3V compatibility).

Selection between both modes is done by SW1 switch:

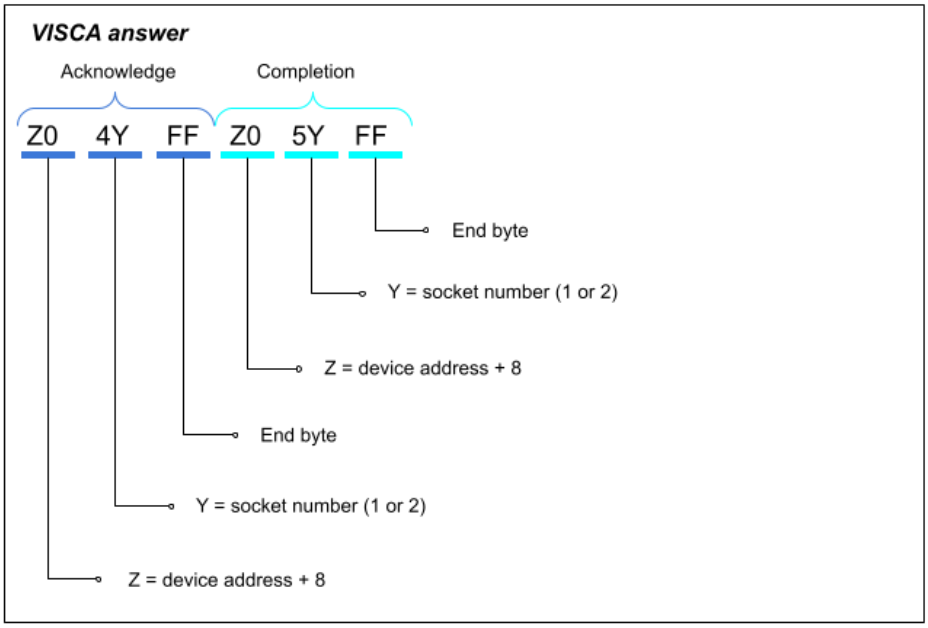
SW1	Configuration
OFF	**RS232**
ON	**TTL**

To the camera

The camera communication uses VISCA protocol and will follow camera specifications. It is a standard protocol for camera blocks following this structure:

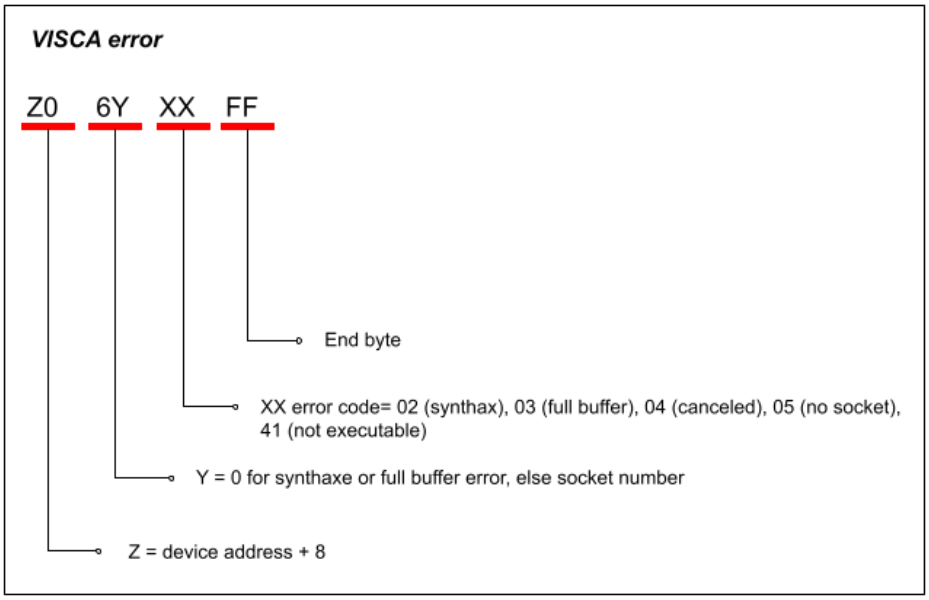


The camera answer follows this structure:



The time between the acknowledgement and the completion packet depends on the command. The answer for an inquiry is Z0 5Y followed by the information requested with FF as end byte.

If an error occurs, here the answer structure:



Example: Zoom In command with a speed of 7 is 0x81 01 04 07 27 FF and the expected answer is 0x90 41 FF followed by 0x90 51 FF.

You can communicate using communication software like Termite or the camera brand communication tool like Sony FCB Control software.

To the internal registers

The board parameters are accessible from the connector J4 with VISCA protocol at Address 0x82.

Register name	Address	Saved	Set command	Comments	Inquiry Command	Inquiry Answer
REG_FPGA_VERSION_H	**0x01**	No	NA	Software version MSB	0x82 09 06 01 FF	0xA0 50 01 00 0y FF
REG_FPGA_VERSION_L	**0x02**	No	NA	Software version LSB	0x82 09 06 02 FF	0xA0 50 02 00 0y FF
REG_FPGA_TEMPERATURE	**0x04**	No	NA	See Annex 1	0x82 09 06 04 FF	0xA0 50 04 0y 0y FF
REG_FPGA_REBOOT	**0x05**	No	0x82 01 06 05 00 01 FF	Reboot the FPGA	NA	NA
REG_FPGA_NB_BOOT_H	**0x07**	No	NA	System boot counter High	0x82 09 06 07 FF	0xA0 50 07 0y 0y FF
REG_FPGA_NB_BOOT_M	**0x08**	No	NA	System boot counter Middle	0x82 09 06 08 FF	0xA0 50 08 0y 0y FF
REG_FPGA_NB_BOOT_L	**0x09**	No	NA	System boot counter Low	0x82 09 06 09 FF	0xA0 50 09 0y 0y FF
REG_FPGA_RUNTIME_H	**0x0A**	No	NA	Runtime High	0x82 09 06 0A FF	0xA0 50 0A 0y 0y FF
REG_FPGA_RUNTIME_MH	**0x0B**	No	NA	Runtime Middle High	0x82 09 06 0B FF	0xA0 50 0B 0y 0y FF
REG_FPGA_RUNTIME_ML	**0x0C**	No	NA	Runtime Middle Low	0x82 09 06 0C FF	0xA0 50 0C 0y 0y FF
REG_FPGA_RUNTIME_L	**0x0D**	No	NA	Runtime Low	0x82 09 06 0D FF	0xA0 50 0D 0y 0y FF
REG_GENNUM_STS_H	**0x10**	No	NA	Gennum status reg 004 MSB	0x82 09 06 10 FF	0xA0 50 10 0y 0y FF
REG_GENNUM_STS_L	**0x11**	No	NA	Gennum status reg 004 LSB	0x82 09 06 11 FF	0xA0 50 11 0y 0y FF
REG_DBG_LED	**0x12**	Yes	0x82 01 06 12 0y 0y FF	0x00: LED OFF 0x01: LED ON	0x82 09 06 12 FF	0xA0 50 12 00 0y FF
REG_CONFIG_SAVE	**0x13**	No	0x82 01 06 13 00 01 FF	Save registers values to flash	NA	NA
REG_CONFIG_LOAD	**0x14**	No	0x82 01 06 14 00 01 FF	Reload registers values from flash	NA	NA
REG_ANALOG_FORMAT	**0x20**	Yes	0x82 01 06 20 00 0y FF	0x00: CVBS / S-Video 0x01: YPbPr	0x82 09 06 20 FF	0xA0 50 20 00 0y FF
REG_SD_FORMAT	**0x21**	Yes	0x82 01 06 21 00 0y FF	0x00: PAL 0x01: NTSC	0x82 09 06 21 FF	0xA0 50 21 00 0y FF
REG_SD_RESIZE	**0x22**	Yes	0x82 01 06 22 00 0y FF	0x01: Letter box 0x02: Squeeze 0x03: Crop	0x82 09 06 22 FF	0xA0 50 22 00 0y FF
REG_PATTERN_ENABLE	**0x23**	No	0x82 01 06 23 00 0y FF	0x00: Disabled 0x01: Enabled	0x82 09 06 23 FF	0xA0 50 23 00 0y FF
REG_Y_PATTERN	**0x24**	Yes	0x82 01 06 24 0y 0y FF	Y value of pattern	0x82 09 06 24 FF	0xA0 50 24 0y 0y FF
REG_CB_PATTERN	**0x25**	Yes	0x82 01 06 25 0y 0y FF	Cb value of pattern	0x82 09 06 25 FF	0xA0 50 25 0y 0y FF
REG_CR_PÄTTERN	**0x26**	Yes	0x82 01 06 26 0y 0y FF	Cr value of pattern	0x82 09 06 26 FF	0xA0 50 26 0y 0y FF
REG_VIDEO_FORMAT	**0x27**	No	NA	See Annex 2	0x82 09 06 27 FF	0xA0 50 27 0y 0y FF
REG_VIDEO_DETECTED	**0x28**	No	NA	0x01: video detected Other: video not detected	0x82 09 06 28 FF	0xA0 50 28 00 0y FF
REG_CAM_VENDOR_ID_H	**0x30**	No	NA	Camera vendor ID MSB	0x82 09 06 30 FF	0xA0 50 30 0y 0y FF
REG_CAM_VENDOR_ID_L	**0x31**	No	NA	Camera vendor ID LSB	0x82 09 06 31 FF	0xA0 50 31 0y 0y FF
REG_CAM_MODEL_ID_H	**0x32**	No	NA	Camera model ID MSB	0x82 09 06 32 FF	0xA0 50 32 0y 0y FF
REG_CAM_MODEL_ID_L	**0x33**	No	NA	Camera model ID LSB	0x82 09 06 33 FF	0xA0 50 33 0y 0y FF
REG_CAM_UART_BYPASS	**0x34**	No	0x82 01 06 34 0A 05 FF	Bypass the communication for camera update *	N/A	N/A
REG_FLASH_SIZE	**0x50**	No	NA	0x10: 16Mb 0x20: 32Mb 0x40: 64Mb	0x82 09 06 50 FF	0xA0 50 50 0y 0y FF

* Note Reg 0x34: The board needs to be restarted after the camera update to enable the communication again. Be sure that your camera can be updated only using the Kel cable (no need to connect any FFC cable).

Control camera video format

Three DIP switches are used to select the video format of the camera. The board checks, when the camera power is on, if the camera video format corresponds to the switches, otherwise it sends a VISCA command to change the format. It can be changed dynamically; the system will automatically detect the format change and display the video in the format requested. An "External" mode is available to use the actual format of the camera, it does not change the video format of the camera.

SW2	SW3	SW4	Configuration
OFF	OFF	OFF	Default camera format
OFF	OFF	ON	1080p30
OFF	ON	OFF	1080p25
OFF	ON	ON	1080p60
ON	OFF	OFF	1080p50
ON	OFF	ON	720p60
ON	ON	OFF	720p50
ON	ON	ON	1080i60

Please note that video formats can depend on the camera model used.

GPIOs

Six GPIOs are available on J901 connector, each one is dedicated to a specific camera function:

Pin	Action	Control	VISCA command sent
Ctrl1	Press Release	Zoom + Zoom stop	0x81 01 04 07 26 FF 0x81 01 04 07 00 FF
Ctrl2	Press Release	Zoom – Zoom stop	0x81 01 04 07 36 FF 0x81 01 04 07 00 FF
Ctrl3	Press Release	Focus Auto / Manual	0x81 01 04 38 10 FF
Ctrl4	Press Release	Focus near Focus stop	0x81 01 04 08 33 FF 0x81 01 04 08 00 FF
Ctrl5	Press Release	Focus far Focus stop	0x81 01 04 08 23 FF 0x81 01 04 08 00 FF
Ctrl6	Press Release	Image freeze toggle	0x81 01 04 62 02 FF 0x81 01 04 62 03 FF

To activate it you need to connect the pin to the ground. ESD filters and anti-bounce have been added. You can use existing keyboard to easily control them.
For the connector pinout please see paragraph Connectors.

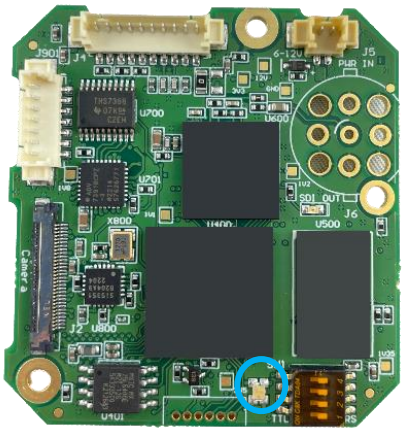
Board Status

The board can be in 4 different states:

- Initialization: the video format and the camera are not detected yet.
- Ready: the board is ready to use, the video format has been detected and the camera is recognized.
- Update: an update is ongoing. The board can easily be updated via UART.
- Error: the video format is not supported. The board goes in this state if the initialization phase fails.

The led color shows in which state the board is:

- Flashing yellow: Video format not detected
- Flashing green: Video format detected
- Flashing blue: Update
- Led can be disabled via register REG_DBG_LED (0x12)



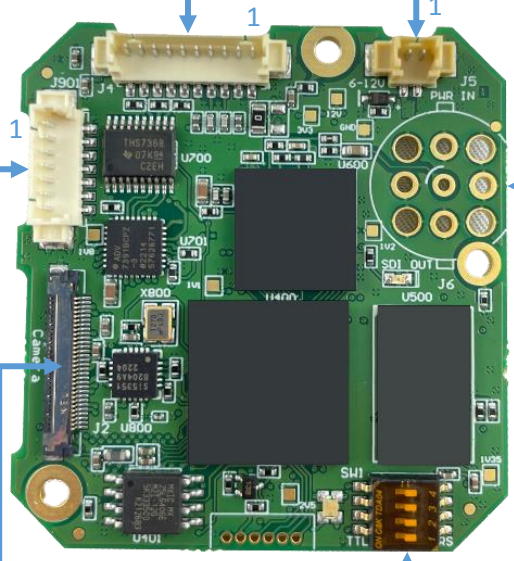
Connectors

J4	Analogue HD/SD output + COM
1	CVBS OUT
2	GND
3	UART-RX
4	UART-TX
5	GND
6	Pr / SC OUT
7	GND
8	Pb / SC OUT
9	GND
10	Y / CVBS OUT

J5	External Power Supply
1	GND
2	7 to 12 VDC

J6	BNC / MCX / SMB compatibility

J901	GPIOs
1	GND
2	Zoom +
3	Zoom -
4	Focus Auto/Manual
5	Focus Near
6	Focus Far
7	Freeze On/Off

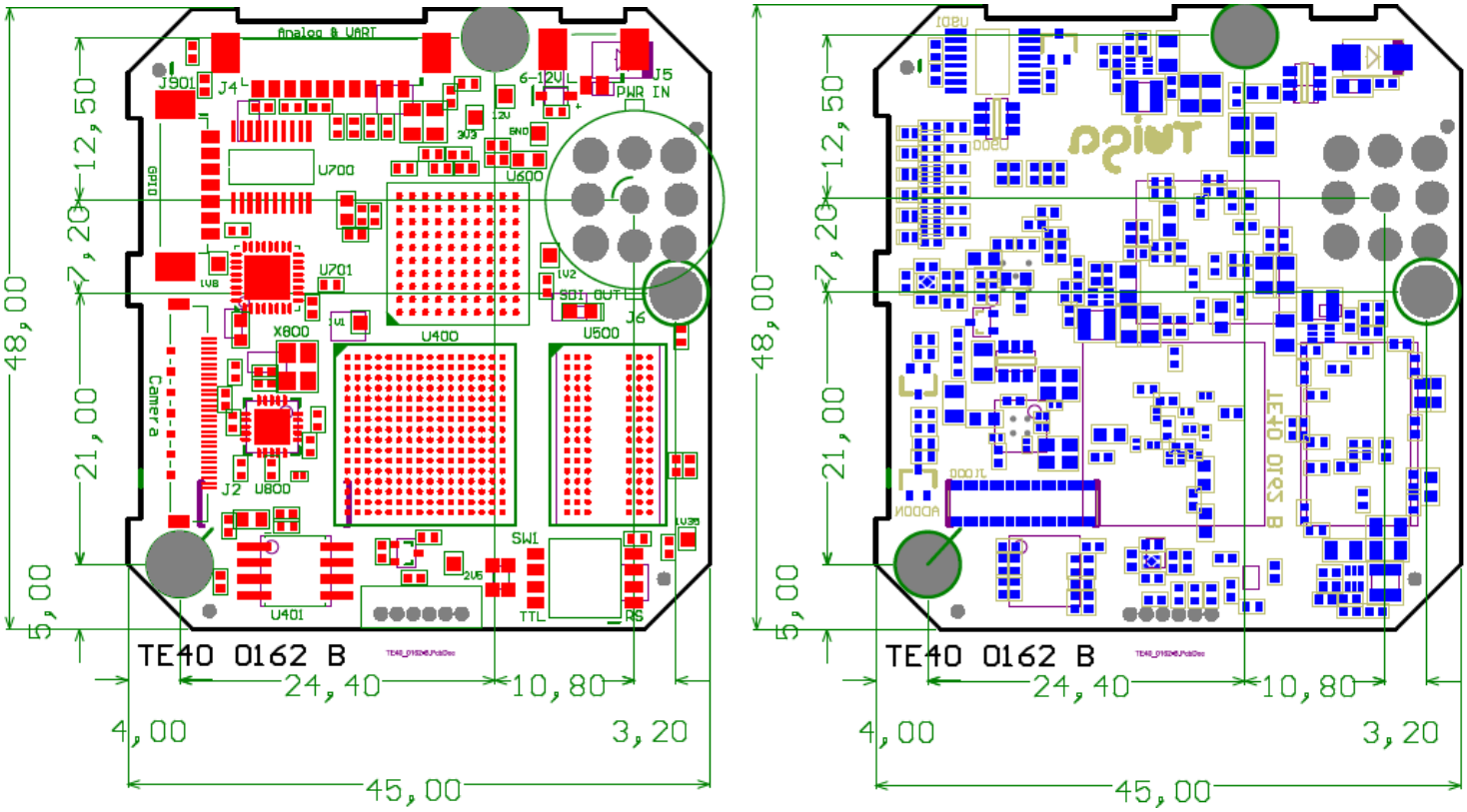


DIP switches				Configuration
1	2	3	4	
OFF	/	/	/	RS232
ON	/	/	/	TTL
/	OFF	OFF	OFF	External
/	OFF	OFF	ON	1080p30
/	OFF	ON	OFF	1080p25
/	OFF	ON	ON	1080p60
/	ON	OFF	OFF	1080p50
/	ON	OFF	ON	720p60
/	ON	ON	OFF	720p50
/	ON	ON	ON	720p30

J2	LVDS input
1	TX4-
2	TX4+
3	TX5-
4	TX5+
5	Reset
6	NC
7	TX6-
8	TX6+
9	TX7-
10	TX7+
11	GND
12	GND
13	VCAM
14	VCAM
15	VCAM
16	VCAM
17	VCAM
18	RxD (TTL camera input)
19	TxD (TTL camera input)
20	GND
21	TX0-
22	TX0+
23	TX1-
24	TX1+
25	TX2-
26	TX2+
27	TXCLKOUT-
28	TXCLKOUT+
29	TX3-
30	TX3+

J1000	Board to board connector
	Extended functionalities

Form factor



TOP BOTTOM

48mm (H) x 45mm (W) x 18mm (D)

4 holes Ø 3mm

15g

Troubleshooting

Get hardware and software version

The hardware version is a letter written close to the reference of the board TV10 0090. The software version is written on a green sticker stuck on the top side of the board. Be careful, the 3G/HD-SDI can be updated by the customer, in this case the green sticker can be not at the correct version. You can still read internal registers to get the correct version.

Update via UART

An update of the board is possible by distance, you need an UART connection with the board and a Java application made by i2S. You can find the application and the different available software version on www.twiga-support.com where a changelog file gives you all the information about the features updated in each version. If you do not have an account on our support website, please register and send us a mail at info@twiga-web.com specifying which board you are working with. This way we will give the rights to have access to our different documentations and software.

Common issues

If you have any problem getting the video, here some points you need to check:

- Power supply is correctly connected to the board, no consuming issue or overheating of the board
- No damaged cable, you can check using other 30-way Kel cable, if possible, check the output cable used to get the video
- Check your display compatibility with the video format you want to read
- The video format of the camera is correct and supported by the board
- The LVDS mode of the camera (register 74) is adapted to your video format: dual mode (value 0x01) for 1080p50, 1080p59.94 and 1080p60, or single mode (value 0x00) for other video formats.
- Try with another LVDS compatible camera to be sure the issue is not coming from the camera
- You can check on our support website that there is no new software version solving your issue

If you are not able to find the cause of the issue, please contact us at info@twiga-web.com and we will give you support. Explain us the problem you are facing with as much details as possible and please add the hardware and software version of your board.

Annex

Annex 1: FPGA temperature table

Here the table to get the FPGA temperature (°C) from the value read in the register 0x04.

Register value read	FPGA temperature (°C)
0x00	–58
0x01	–56
0x02	–54
0x03	–52
0x04	–45
0x05	–44
0x06	–43
0x07	–42
0x08	–41
0x09	–40
0x0A	–39
0x0B	–38
0x0C	–37
0x0D	–36
0x0E	–30
0x0F	–20
0x10	–10
0x11	–4
0x12	0
0x13	4
0x14	10
0x15	21
0x16	22
0x17	23
0x18	24
0x19	25
0x1A	26
0x1B	27
0x1C	28
0x1D	29
0x1E	40
0x1F	50
0x20	60
0x21	70
0x22	76
0x23	80
0x24	81
0x25	82
0x26	83
0x27	84
0x28	85
0x29	86
0x2A	87
0x2B	88
0x2C	89

0x2D	95
0x2E	96
0x2F	97
0x30	98
0x31	99
0x32	100
0x33	101
0x34	102
0x35	103
0x36	104
0x37	105
0x38	106
0x39	107
0x3A	108
0x3B	116
0x3C	120
0x3D	124
0x3E	128
0x3F	132

Annex 2: Video format table

Here the table to get the video format from the value read in the register 0x27.

Register value read	Video format
0x00	No video
0x01	Unknown
0x20	720p25
0x21	720p29,97
0x22	720p30
0x23	720p50
0x24	720p59,94
0x25	720p60
0x26	1080i50
0x27	1080i59,94
0x28	1080i60
0x29	1080p25
0x2A	1080p29,97
0x2B	1080p30
0x40	1080p50
0x41	1080p59,94
0x42	1080p60