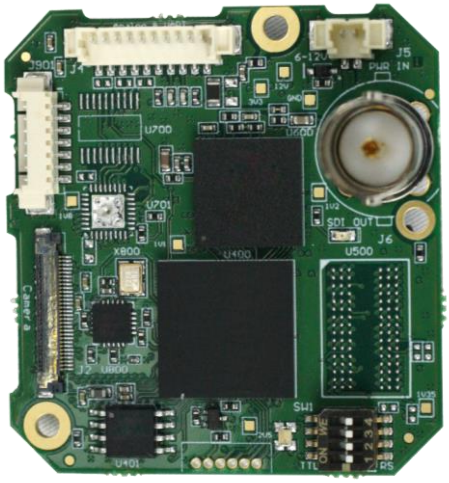
Vision & Innovation

3G/HD-SDI Neo

Technical Manual



P/N – TV10 0096: 3G/HD-SDI **Neo** interface board for LVDS zoom cameras

P/N – TV50 0020: Mounting kit for TV10 0096 – 3G/HD-SDI Neo I/F board
Includes: 30-way micro-coax camera cable, 2-way cable (power supply), 10-way cable (RS232/TTL/Analog output), 7-way cable (GPIOs), right angle black anodized bracket, screws and spacers

P/N – TV50 0021: Cable kit for TV10 0096 – 3G/HD-SDI Neo I/F board
Includes: 30-way micro-coax camera cable, 2-way cable (power supply), 10-way cable (RS232/TTL/Analog output)

Available connectors: Default (BNC), VOPTEM02 (MCX connector), VOPTEM03 (SMB connector), VOPTEM04 (No connector)

Table of content

Revision History

Date	Revision	Description	Modified by	Note
07/02/23	A	Creation of the document	CBO	
19/01/24	B	Document refactoring	CBO	
12/06/24	C	Add REG_CAM_UART_BYPASS Change DIP switch video format	CBO	
28/02/25	D	Change document graphical chart	CBO	
08/10/25	E	Add GPIO management part and progressive to interlaced conversion registers	CBO	

Key features

- 3G-SDI SMPTE 424M, HD-SDI 292 M
- Video resolution up to 1080p60
- Ultra-low transmission latency (< 1ms)
- Communication UART – RS232/TTL using VISCA
- Setup & Update via UART
- Video mode selection by DIP switches
- Power supply 7V-12VDC
- Consumption under 6W with camera
- Automatic LVDS & format camera recognition
- Add-on connector for custom functionalities
- Operating temperature [0°C; 60°C]

General description

3G-SDI technology is the first established standard providing sufficient bandwidth to transmit uncompressed high-definition video signals from camera to screen.

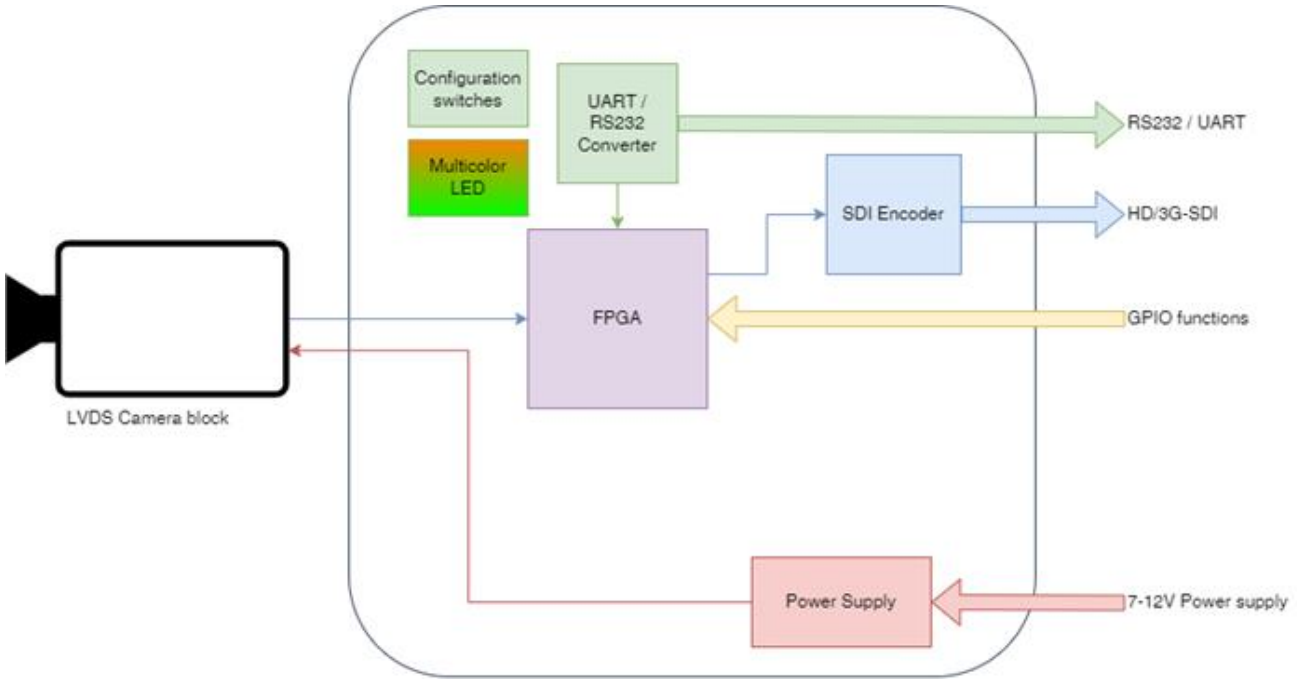
Using coaxial cables with very low power loss, enables video transmission over 100 meters. This distance can be increased up to 300 meters using equalization at the receiver.
The 3G-SDI Neo converts the native LVDS video signal from camera blocks to 3G-SDI. It takes advantage of a high quality, low jitter, and uncompressed SDI stream.

The add-on connector on the back side offers an infinity of new functionalities. The 3G-SDI Neo can be directly mounted into your system/end-products (plug-in) or connected to custom designed add-on board. Integrated RTC, audio embedded to SDI, second video input are some examples of the new possibilities / range of functionalities.

Benefits of this solution

- Standard and reliable SDI video transmission
- Up to 1080p60
- Latency involved by the board is negligible
- RS232 / TTL serial communication easy switch
- Always keep up to date with an easy software update
- Addon connector for custom needs
- 3G SDI output connector choice between BNC, MCX and SMB
- GPIOs connector to easily send basic VISCA commands (zoom in / out, freeze on / off, focus)

Block diagram



Video acquisition

The main component is the FPGA for video acquisition.
The board acquire LVDS video from the camera block with no latency deserialization to provide uncompressed 3G-SDI video output via an SDI converter.

Communication

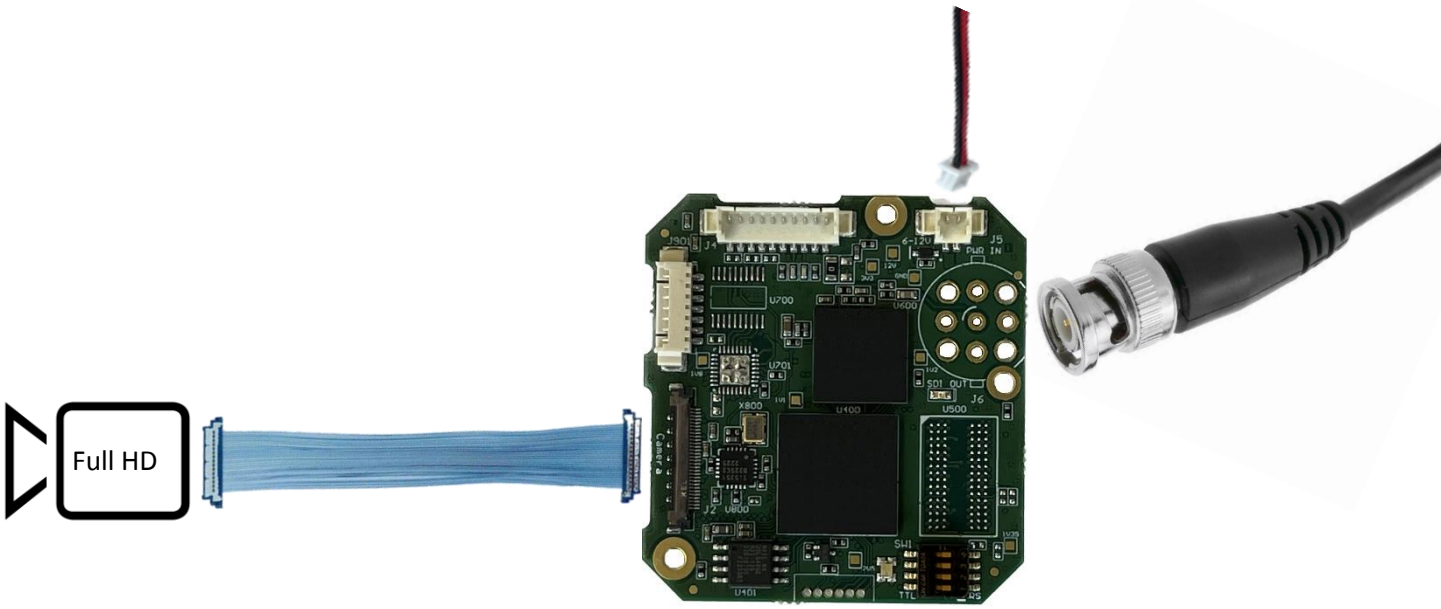
An UART / RS232 converter allows the user to select RS232 or UART TTL 3V3 communication. It is easily selectable via a DIP switch.
The DIP switch is used to manage the camera video format too.
A multicolor LED helps to know in which state the board is, it is quick feedback to be sure no error happened.

Power supply

The power input through the 2-way connector J5 supports from 7V to 12V (1,5A). The camera is powered by the board.
The board is protected against shortcut and reversed cables.

Accessing the video

Quick setup



Installation steps:

1. Connect the KEL cable between the board J2 and the camera.
2. Connect the SDI cable to the output connector of the board J6 and to the SDI monitor.
3. Connect the 2-way power supply cable on J5 connector. Power input of the board is 7V to 12V (1,5A), red wire is for V+ and black wire is for the ground.
4. Now you can power the board.

Video characteristics

Introduction on video formats

You have two video format types:

- Progressive: displays both the even and odd scan lines (the entire video frame) at the same time. The video formats are listed with the letter 'p'.
- Interlaced: displays even and odd scan lines as separate fields. The even scan lines are drawn on the screen, then the odd scan lines are drawn on the screen. Two of these even and odd scan line fields make up one video frame. The video formats are listed with the letter 'i'.

Notion of LVDS mode:

- It is controlled by the register 74 of the camera (0x00: Single mode, 0x01: Dual mode).
- It is used to increase the video output from 4x LVDS data lines to 8x LVDS data lines. The output clock frequency is still 74,25MHz but with twice more date lanes.
- It is needed to process video formats 1080p50, 1080p59.94 and 1080p60. If the camera itself does not have 4x additional LVDS data lanes, it will output data at 148,5MHz for video formats 1080p50, 1080p59.94 and 1080p60.

On LVDS Full HD cameras blocks you can have several video formats available:

- Full HD Interlaced 1920x1080i: it can be at 50, 59.94 or 60 FPS, the camera must be in Single mode.
- Full HD Progressive 1920x1080p: it can be at 25, 29.97 or 30 FPS, the camera must be in Single mode. It can also be at 50, 59.94 or 60 FPS, with these video formats only, the camera must be in Dual mode to be able to send more data.
- HD Progressive 1280x720p: it can be at 25, 29.97, 30, 50, 59.94 or 60 FPS, the camera must be in single mode.

LVDS video input supported resolutions

The video format from the LVDS camera can be configured by sending VISCA command using the register 72.

	25	29.97	30	50	59.94	60
1280x720p	✓	✓	✓	✓	✓	✓
1920x1080p	✓	✓	✓	✓*	✓*	✓*
1920x1080i				✓	✓	✓

* The video formats 1080p50, 1080p59.94 and 1080p60 require the camera configured in dual lane: register 74 set to 0x01. The others video formats require the register 74 set to 0x00 for single lane.

SDI video output

The output is an 8-bit SDI signal 800mV pp with 75-ohm impedance. It is compliant with SMPTE 424M (3G-SDI) and SMPTE 292M (HD-SDI). The output video format is the same as the camera (see LVDS video input resolutions supported upper).
Different output connector types are available: BNC, SMB or MCX. Please specify the connector you need in the order.

BNC  MCX  SMB 

System configuration

Communication

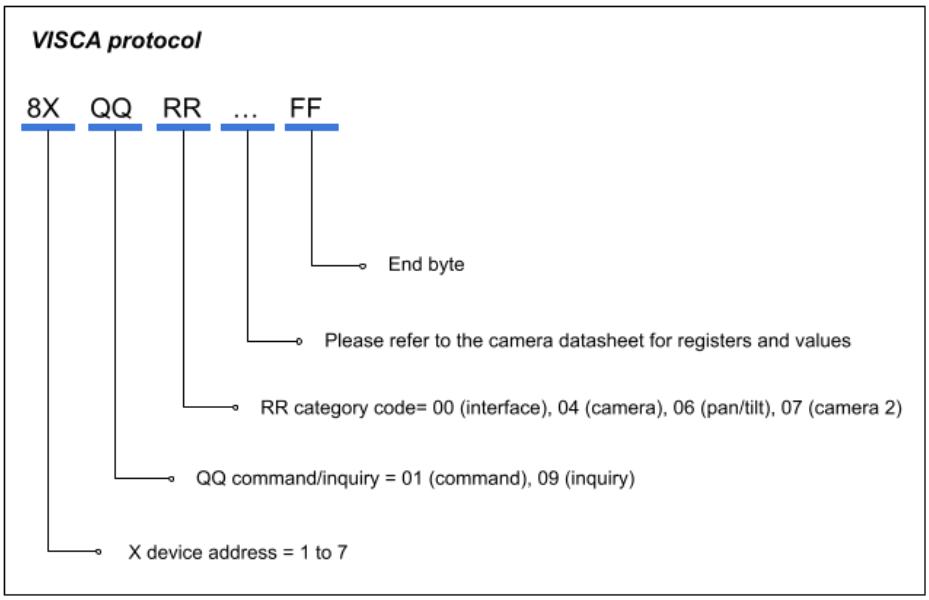
Communication with the camera can be done through J4 connector.

It can be set to either RS232 mode (according to EIA RS-232 specification) or TTL mode (UART with 3.3V compatibility).
Selection between both modes is done by SW1 switch:

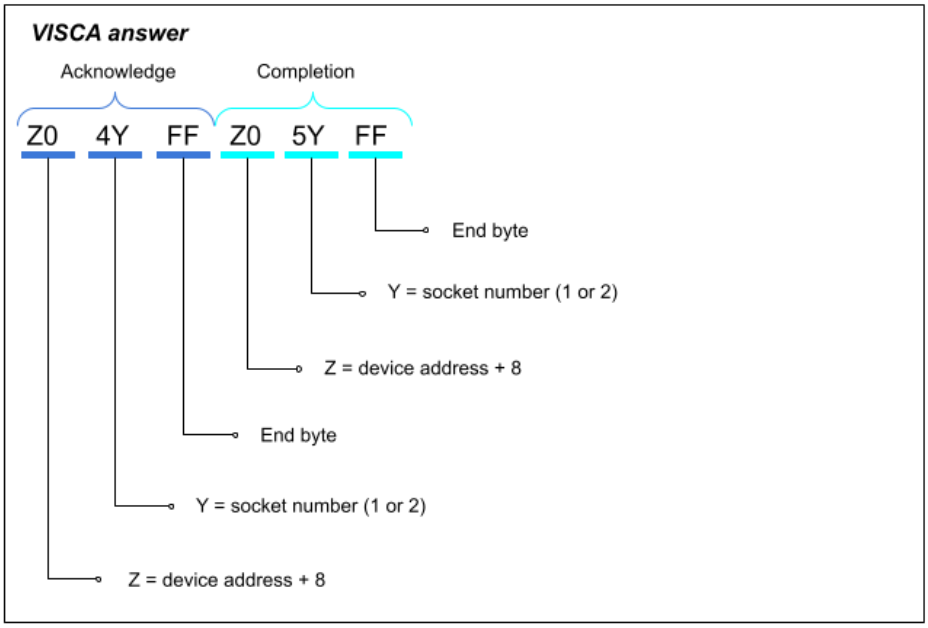
SW1	Configuration
OFF	RS232
ON	TTL

To the camera

The camera communication uses VISCA protocol and will follow camera specifications. It is a standard protocol for camera blocks following this structure:

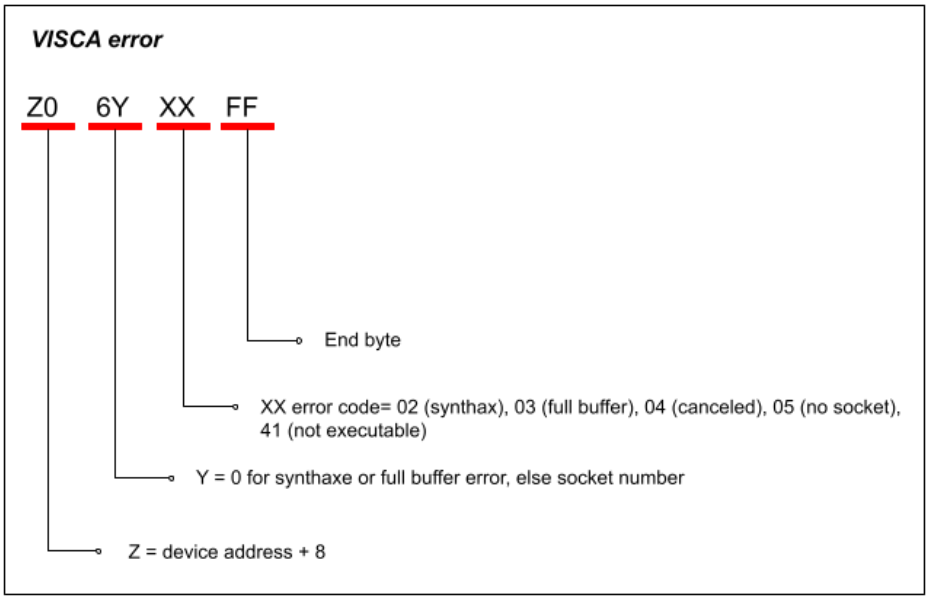


The camera answer follows this structure:



The time between the acknowledgement and the completion packet depends on the command. The answer for an inquiry is Z0 5Y followed by the information requested with FF as end byte.

If an error occurs, here the answer structure:



Example: Zoom In command with a speed of 7 is 0x81 01 04 07 27 FF and the expected answer is 0x90 41 FF followed by 0x90 51 FF.

You can communicate using communication software like Termite or the camera brand communication tool like Sony FCB Control software.

To the internal registers

The board parameters are accessible from the connector J4 with VISCA protocol at Address 0x82.

Register name	Addr	Saved	Set command	Comments	Inquiry command	Inquiry answer
REG_FPGA_VERSION_H	0x01	No	NA	Software version MSB	0x82 09 06 01 FF	0xA0 50 01 00 0y FF
REG_FPGA_VERSION_L	0x02	No	NA	Software version LSB	0x82 09 06 02 FF	0xA0 50 02 00 0y FF
REG_FPGA_VERSION_MIC	0x03	No	NA	Software version micro	0x82 09 06 03 FF	0xA0 50 03 0y 0y FF
REG_FPGA_TEMPERATURE	0x04	No	NA	See Annex 1	0x82 09 06 04 FF	0xA0 50 04 0y 0y FF
REG_FPGA_REBOOT	0x05	No	0x82 01 06 05 00 01 FF	Reboot the FPGA	NA	NA
REG_FPGA_NB_BOOT_H	0x07	No	NA	Boot counter High	0x82 09 06 07 FF	0xA0 50 07 0y 0y FF
REG_FPGA_NB_BOOT_M	0x08	No	NA	Boot counter Middle	0x82 09 06 08 FF	0xA0 50 08 0y 0y FF
REG_FPGA_NB_BOOT_L	0x09	No	NA	Boot counter Low	0x82 09 06 09 FF	0xA0 50 09 0y 0y FF
REG_FPGA_RUNTIME_H	0x0A	No	NA	Runtime High	0x82 09 06 0A FF	0xA0 50 0A 0y 0y FF
REG_FPGA_RUNTIME_MH	0x0B	No	NA	Runtime Middle High	0x82 09 06 0B FF	0xA0 50 0B 0y 0y FF
REG_FPGA_RUNTIME_ML	0x0C	No	NA	Runtime Middle Low	0x82 09 06 0C FF	0xA0 50 0C 0y 0y FF
REG_FPGA_RUNTIME_L	0x0D	No	NA	Runtime Low	0x82 09 06 0D FF	0xA0 50 0D 0y 0y FF
REG_GENNUM_STS_H	0x10	No	NA	Gennum status reg 004 MSB	0x82 09 06 10 FF	0xA0 50 10 0y 0y FF
REG_GENNUM_STS_L	0x11	No	NA	Gennum status reg 004 LSB	0x82 09 06 11 FF	0xA0 50 11 0y 0y FF
REG_DBG_LED	0x12	Yes	0x82 01 06 12 0y 0y FF	0x00: LED OFF 0x01: LED ON	0x82 09 06 12 FF	0xA0 50 12 00 0y FF
REG_CONFIG_SAVE	0x13	No	0x82 01 06 13 00 01 FF	Save registers values to flash	NA	NA
REG_CONFIG_LOAD	0x14	No	0x82 01 06 14 00 01 FF	Reload registers values from flash	NA	NA
REG_PATTERN_ENABLE	0x23	No	0x82 01 06 23 00 0y FF	0x00: Disabled 0x01: Enabled	0x82 09 06 23 FF	0xA0 50 23 00 0y FF
REG_Y_PATTERN	0x24	Yes	0x82 01 06 24 0y 0y FF	Y value of pattern	0x82 09 06 24 FF	0xA0 50 24 0y 0y FF
REG_CB_PATTERN	0x25	Yes	0x82 01 06 25 0y 0y FF	Cb value of pattern	0x82 09 06 25 FF	0xA0 50 25 0y 0y FF
REG_CR_PATTERN	0x26	Yes	0x82 01 06 26 0y 0y FF	Cr value of pattern	0x82 09 06 26 FF	0xA0 50 26 0y 0y FF
REG_VIDEO_FORMAT	0x27	No	NA	See Annex 2	0x82 09 06 27 FF	0xA0 50 27 0y 0y FF
REG_VIDEO_DETECTED	0x28	No	NA	0x01: video detected Other: video not detected	0x82 09 06 28 FF	0xA0 50 28 00 0y FF
REG_INTERLACED_N	0x29	Yes	0x82 01 06 29 0y 0y FF	0x00: progressive to interlaced conversion ON 0x01: conversion OFF*	0x82 09 06 29 FF	0xA0 50 29 00 0y FF
REG_CAM_VENDOR_ID_H	0x30	No	NA	Camera vendor ID MSB	0x82 09 06 30 FF	0xA0 50 30 0y 0y FF
REG_CAM_VENDOR_ID_L	0x31	No	NA	Camera vendor ID LSB	0x82 09 06 31 FF	0xA0 50 31 0y 0y FF
REG_CAM_MODEL_ID_H	0x32	No	NA	Camera model ID MSB	0x82 09 06 32 FF	0xA0 50 32 0y 0y FF
REG_CAM_MODEL_ID_L	0x33	No	NA	Camera model ID LSB	0x82 09 06 33 FF	0xA0 50 33 0y 0y FF
REG_CAM_UART_BYPASS	0x34	No	0x82 01 06 34 0A 05 FF	Bypass the communication for camera update **	N/A	N/A

Register name	Addr	Saved	Set command	Comments	Inquiry command	Inquiry answer
REG_GPIO_STATE	0x40	Yes	0x82 01 06 40 0y 0y FF	yy = 0b00xxxxxx (x=0 for output, x=1 for input)	0x82 09 06 40 FF	0xA0 50 40 0y 0y FF
REG_GPIO_OUTPUT	0x41	Yes	0x82 01 06 41 0y 0y FF	yy = 0b00xxxxxx (x=0 for < 200mV, x=1 for = 3V3)	0x82 09 06 41 FF	0xA0 50 41 0y 0y FF
REG_GPIO_INPUT	0x42	No	NA	yy = 0b00xxxxxx (x=0 for < 200mV, x=1 for = 3V3)	0x82 09 06 42 FF	0xA0 50 42 0y 0y FF
REG_GPIO_1_CMD	0x43	Yes	0x82 01 06 43 0y 0y FF	VISCA command to send to the camera in input mode ***	0x82 09 06 43 FF	0xA0 50 43 0y 0y FF
REG_GPIO_2_CMD	0x44	Yes	0x82 01 06 44 0y 0y FF	VISCA command to send to the camera in input mode ***	0x82 09 06 44 FF	0xA0 50 44 0y 0y FF
REG_GPIO_3_CMD	0x45	Yes	0x82 01 06 45 0y 0y FF	VISCA command to send to the camera in input mode ***	0x82 09 06 45 FF	0xA0 50 45 0y 0y FF
REG_GPIO_4_CMD	0x46	Yes	0x82 01 06 46 0y 0y FF	VISCA command to send to the camera in input mode ***	0x82 09 06 46 FF	0xA0 50 46 0y 0y FF
REG_GPIO_5_CMD	0x47	Yes	0x82 01 06 47 0y 0y FF	VISCA command to send to the camera in input mode ***	0x82 09 06 47 FF	0xA0 50 47 0y 0y FF
REG_GPIO_6_CMD	0x48	Yes	0x82 01 06 48 0y 0y FF	VISCA command to send to the camera in input mode ***	0x82 09 06 48 FF	0xA0 50 48 0y 0y FF

* Note: The progressive to interlaced conversion works only for input formats: 1080p50/59.94/60.

** Note: The board needs to be restarted after the camera update to enable the communication again. Be sure that your camera can be updated only using the Kel cable (no need to connect any FFC cable).

*** Note: In input configuration the GPIOs are active low and output value is not taken into account. Here the VISCA commands you can select to be sent when the GPIO is activated:

Configuration	Action	Control	VISCA command
0x00: Zoom In	Press Release	Zoom In Zoom Stop	0x81 01 04 07 02 FF 0x81 01 04 07 00 FF
0x01: Zoom Out	Press Release	Zoom Out Zoom Stop	0x81 01 04 07 03 FF 0x81 01 04 07 00 FF
0x02: Zoom In variable speed	Press Release	Zoom In variable speed (Y) Zoom Stop	0x81 01 04 07 2Y FF 0x81 01 04 07 00 FF
0x03: Zoom Out variable speed	Press Release	Zoom Out variable speed (Y) Zoom Stop	0x81 01 04 07 3Y FF 0x81 01 04 07 00 FF
0x04: Focus switch Manual / Auto	Press Release	Focus switch Manual / Auto	0x81 01 04 38 10 FF
0x05: Focus one push	Press Release	Focus one push	0x81 01 04 18 01 FF
0x06: Focus far	Press Release	Focus Far Focus Stop	0x81 01 04 08 02 FF 0x81 01 04 08 00 FF
0x07: Focus near	Press Release	Focus Near Focus Stop	0x81 01 04 08 03 FF 0x81 01 04 08 00 FF
0x08: Freeze toggle	Press Release	Freeze toggle	0x81 01 04 62 0Y FF (Y=2 for ON, Y=3 for OFF)
0x09: Mirror toggle	Press Release	Mirror toggle	0x81 01 04 61 0X FF (Y=2 for ON, Y=3 for OFF)
0x0A: Flip toggle	Press Release	Flip toggle	0x81 01 04 66 0Y FF (Y=2 for ON, Y=3 for OFF)

0x0B: Mute toggle	Press Release	Mute toggle	0x81 01 04 75 10 FF
0x0C: Memory preset	Short press Pressed more than 1 second	Memory preset Recall Memory preset Set	0x81 01 04 3F 02 0Y FF 0x81 01 04 3F 01 0Y FF with Y corresponding to the preset number (set at the GPIO number)
0XFF: No command sent	Press Release	Nothing	Nothing

Examples:

- Use GPIO 1 as input for Freeze toggle: input is the default configuration, send the command 0x82 01 06 43 00 08 FF to attribute the function and save command 0x82 01 06 13 00 01 FF.

- Use GPIO 3 as input for polling only: input is the default configuration, send the command 0x82 01 06 45 0F 0F FF to attribute no function avoiding sending VISCA command to the camera when the GPIO is active, and save command 0x82 01 06 13 00 01 FF.
  Polling is done by reading register REG_GPIO_INPUT with this command 0x82 09 06 42 FF. Each GPIO value is read in a bit of the answer: 0xA0 50 42 0y 0y FF with yy = 0b00xxxxxx.

- Use GPIO 5 as output: send command 0x82 01 06 40 02 0F FF (0x2F = 0b00101111, will configure GPIO 5 as output and the others as inputs) and save command 0x82 01 06 13 00 01 FF.
  Set output level: send command 0x82 01 06 41 0y 0y FF with yy = 0b00010000 for GPIO 5 high level (3V3) and yy = 0b00000000 for GPIO 5 low level (0V) and save if needed.

Control camera video format

Three DIP switches are used to select the video format of the camera. The board checks, when the camera power is on, if the camera video format corresponds to the switches, otherwise it sends a VISCA command to change the format. It can be changed dynamically; the system will automatically detect the format change and display the video in the format requested. An "External" mode is available to use the actual format of the camera, it does not change the video format of the camera.

SW2	SW3	SW4	Configuration
OFF	OFF	OFF	Default camera format
OFF	OFF	ON	1080p30
OFF	ON	OFF	1080p25
OFF	ON	ON	1080p60
ON	OFF	OFF	1080p50
ON	OFF	ON	720p60
ON	ON	OFF	720p50
ON	ON	ON	1080i60

Please note that video formats can depend on the camera model used.

GPIOs

Six GPIOs are available on J901 connector, please find bellow their default input configuration which can be changed using internal registers:

Pin	Action	Control
GPIO 1	Press Release	Zoom + Zoom stop
GPIO 2	Press Release	Zoom – Zoom stop
GPIO 3	Press Release	Focus Auto / Manual
GPIO 4	Press Release	Focus near Focus stop
GPIO 5	Press Release	Focus far Focus stop
GPIO 6	Press Release	Image freeze toggle

To activate it you need to connect the pin to the ground. ESD filters and anti-bounce have been added. You can use existing keyboard to easily control them.

Please note that in output state, the low level is <200mV and high level is 3V3.

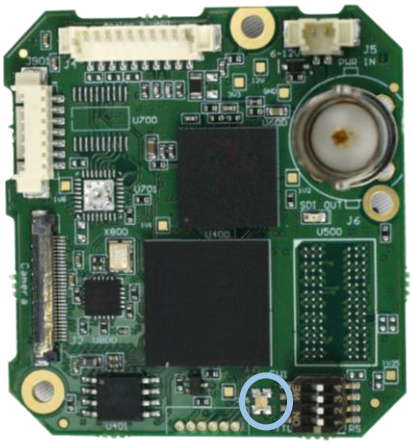
Board status

The board can be in 4 different states:

- Initialization: the video format and the camera are not detected yet.
- Ready: the board is ready to use, the video format has been detected and the camera is recognized.
- Update: an update is ongoing. The board can easily be updated via UART.
- Error: the video format is not supported. The board goes in this state if the initialization phase fails.

The led color shows in which state the board is:

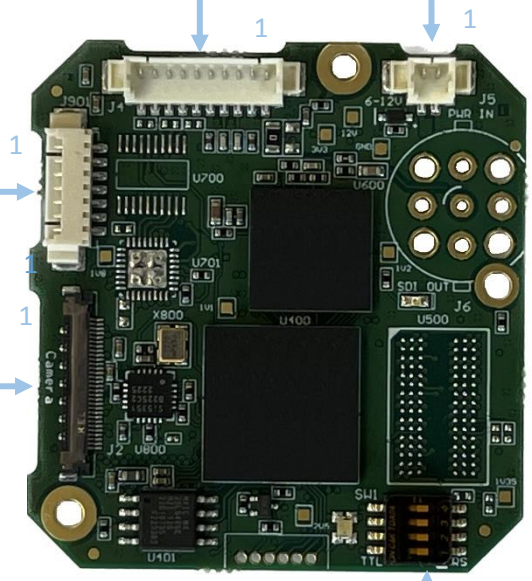
- Flashing yellow: Video format not detected
- Flashing green: Video format detected
- Flashing blue: Update
- Led can be disabled via register REG_DBG_LED (0x12)



Connectors

J4	Communication
1	NA
2	GND
3	Rx
4	Tx
5	GND
6	NA
7	GND
8	NA
9	GND
10	NA

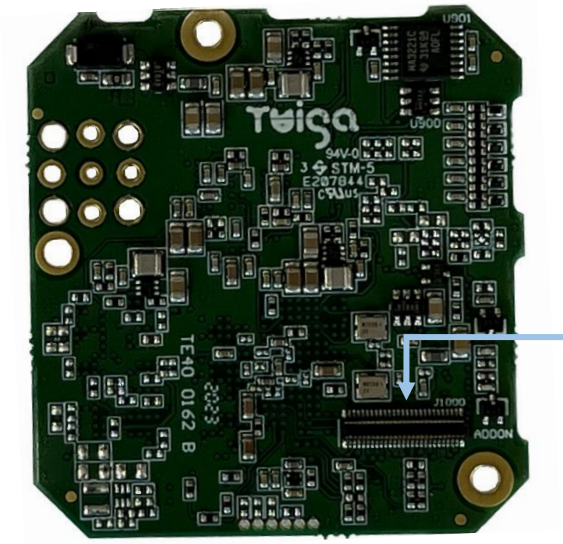
J5	Power supply
1	GND
2	7 to 12 VDC



J901	GPIOs (configurable)
1	GND
2	Zoom +
3	Zoom -
4	Focus Auto/Manual
5	Focus Near
6	Focus Far
7	Freeze On/Off

J6	BNC / MCX / SMB compatibility

J2	LVDS input
1	TX4-
2	TX4+
3	TX5-
4	TX5+
5	Reset
6	NC
7	TX6-
8	TX6+
9	TX7-
10	TX7+
11	GND
12	GND
13	VCAM
14	VCAM
15	VCAM
16	VCAM
17	VCAM
18	RxD (TTL camera input)
19	TxD (TTL camera input)
20	GND
21	TX0-
22	TX0+
23	TX1-
24	TX1+
25	TX2-
26	TX2+
27	TXCLKOUT-
28	TXCLKOUT+
29	TX3-
30	TX3+

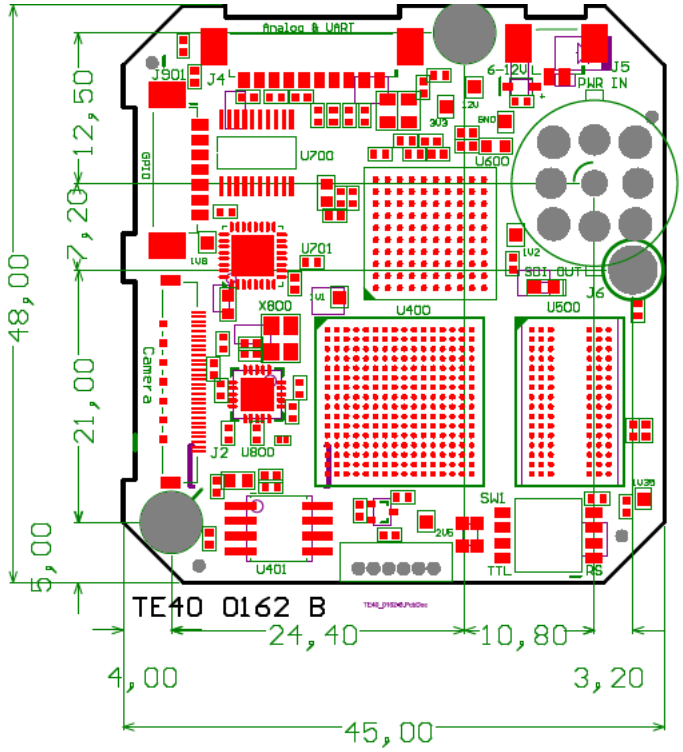


DIP switches				Configuration
1	2	3	4	
OFF	/	/	/	RS232
ON	/	/	/	UART TTL
/	OFF	OFF	OFF	External
/	OFF	OFF	ON	1080p30
/	OFF	ON	OFF	1080p25
/	OFF	ON	ON	1080p60
/	ON	OFF	OFF	1080p50
/	ON	OFF	ON	720p60
/	ON	ON	OFF	720p50
/	ON	ON	ON	1080i60

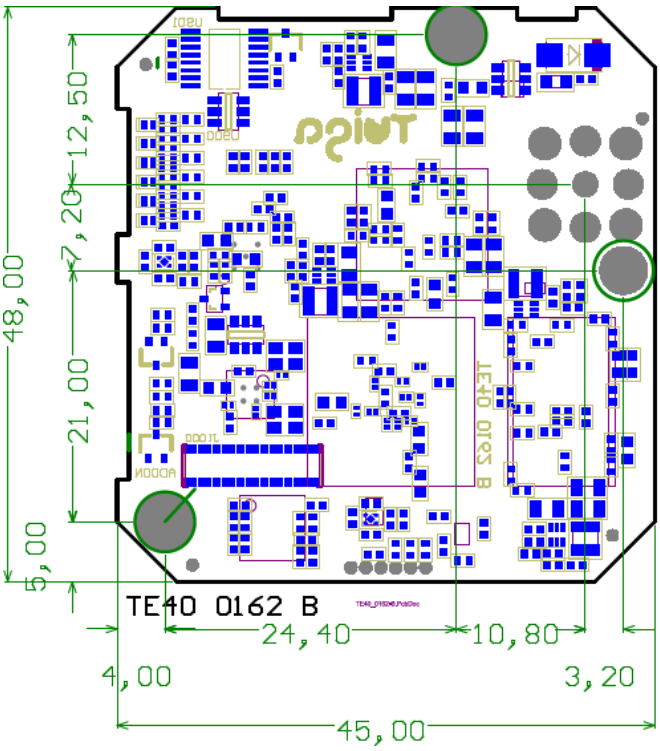
J1000	Board to Board connector
Extended functionalities	

Form factor

TOP



BOTTOM



48mm (H) x 45mm (W) x 18mm (D)

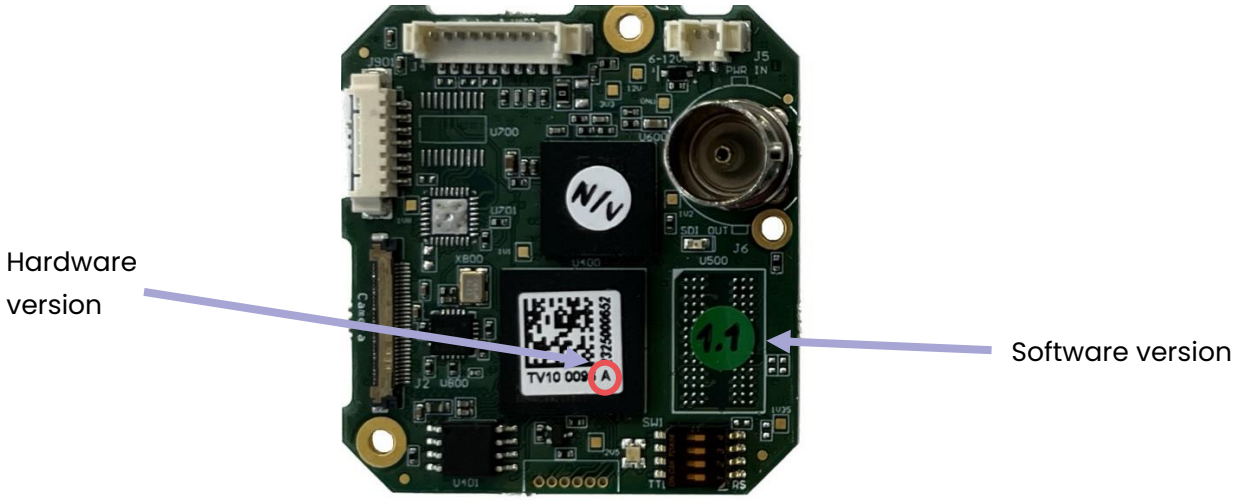
4 holes Ø 3mm

15g

Troubleshooting

Get hardware and software version

The hardware version is a letter written close to the reference of the board TV10 0096. The software version is written on a green sticker stuck on the top side of the board. Be careful, 3G/HD-SDI Neo can be updated by the customer, in this case the green sticker could be at a wrong version. You can still read internal registers to get the correct version.



Update via UART

An update of the board is possible by distance, you need an UART connection with the board and a Java application made by i2S.
If you do not have this tool, please send us a mail at info@i2s.fr specifying which board you are working with. This way we will give you the right tool to perform the software update and the changes involved by the different software.

Common issues

If you have any problem getting the video, here some points you need to check:

- Power supply is correctly connected to the board, no consuming issue or overheating of the board.
- No damaged cable, you can check using other 30-way Kel cable, if possible, check the output cable used to get the video
- Check your display compatibility with the video format you want to read
- The video format of the camera is correct and supported by the board
- The LVDS mode of the camera (register 74) is adapted to your video format: dual mode (value 0x01) for 1080p50, 1080p59.94 and 1080p60, or single mode (value 0x00) for other video formats.
- Try with another LVDS compatible camera to be sure the issue is not coming from the camera

If you are not able to find the cause of the issue, please contact us at info@i2s.fr and we will give you support. Explain us the problem you are facing with as much details as possible and please add the hardware and software version of your board.

Annex

Annex 1: FPGA temperature table

Here the table to get the FPGA temperature (°C) from the value read in the register 0x04.

Register value read	FPGA temperature (°C)
0x00	−58
0x01	−56
0x02	−54
0x03	−52
0x04	−45
0x05	−44
0x06	−43
0x07	−42
0x08	−41
0x09	−40
0x0A	−39
0x0B	−38
0x0C	−37
0x0D	−36
0x0E	−30
0x0F	−20
0x10	−10
0x11	−4
0x12	0
0x13	4
0x14	10
0x15	21
0x16	22
0x17	23
0x18	24
0x19	25
0x1A	26
0x1B	27
0x1C	28
0x1D	29
0x1E	40
0x1F	50
0x20	60
0x21	70
0x22	76
0x23	80
0x24	81
0x25	82
0x26	83
0x27	84
0x28	85
0x29	86
0x2A	87
0x2B	88
0x2C	89
0x2D	95

0x2E	96
0x2F	97
0x30	98
0x31	99
0x32	100
0x33	101
0x34	102
0x35	103
0x36	104
0x37	105
0x38	106
0x39	107
0x3A	108
0x3B	116
0x3C	120
0x3D	124
0x3E	128
0x3F	132

Annex 2: Video format table

Here the table to get the video format from the value read in the register 0x27.

Register value read	Video format
0x00	No video
0x01	Unknown
0x20	720p25
0x21	720p29,97
0x22	720p30
0x23	720p50
0x24	720p59,94
0x25	720p60
0x26	1080i50
0x27	1080i59,94
0x28	1080i60
0x29	1080p25
0x2A	1080p29,97
0x2B	1080p30
0x40	1080p50
0x41	1080p59,94
0x42	1080p60